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DESCRIPTION

RECEIVING APPARATUS AND RECEPTION TIMING ESTIMATION
METHOD

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Technical Field

The present invention relates to a receiving apparatus and reception timing estimation method for use in a base station apparatus of a CDMA mobile communication system or the like.

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Background Art

In a mobile communication system, a signal transmitted by radio is received at a receiving apparatus as signals on a plurality of paths for which reception timings differ due to being reflected by reflective bodies on the radio propagation path.

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The CDMA method, which is one kind of multiple-access method, is characterized by being able to estimate the reception timing of each path based on a delay profile, separate the signals received via the various paths, and perform RAKE combination. For this reason, the CDMA method is attracting attention due to its ability to perform high-quality reception even in a multipath environment, and to increase channel capacity.

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The configuration of a conventional CDMA receiving apparatus will be described below using the block diagram shown in FIG.1.

A matched filter 11 detects the correlation between an input signal and a user-specific spreading code. The correlation value detected by the matched filter 11 is input to a delay profile creator 12, a channel estimate calculator 13, and a RAKE combiner 14.

The delay profile creator 12 estimates the reception timing for each path by threshold value determination with respect to the correlation value, and outputs a signal indicating the reception timing of each path to the channel estimate calculator 13 and RAKE combiner 14.

The channel estimate calculator 13 calculates a channel estimate h_a for each path, and outputs a channel estimate conjugate complex number h_a^* to the RAKE combiner 14.

The RAKE combiner 14 multiplies the correlation value by the channel estimate conjugate complex number h_a^* to compensate for channel fluctuations, and performs RAKE combination in symbol units based on the reception timing of each path, thereby improving quality. The RAKE combiner 14 then outputs symbols after RAKE combination to a discrimination circuit 15.

The discrimination circuit 15 makes a hard decision with respect to each despread signal, and outputs demodulated symbols.

In this way, a conventional receiving apparatus outputs demodulated symbols by estimating the reception timing of each path based on a delay profile, separating signals received via various paths, performing RAKE

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FIG.6 is a block diagram showing the internal configuration of the despreading section of a receiving apparatus according to Embodiment 3 of the present invention.

Best Mode for Carrying out the Invention

With reference now to the attached drawings, embodiments of the present invention will be explained in detail below.

(Embodiment 1)

FIG.2 is a block diagram showing the configuration of a receiving apparatus according to Embodiment 1 of

the present invention.

A switch 101 selects a received signal or a signal output from a subtracter 111 as an input signal, and outputs it to a delayer 102 and despreading sections 103-1 to n.

The delayer 102 removes the pilot symbol part from the signal selected by the switch 101, delays it by a predetermined time, and outputs it to the subtracter 111.

Each despreading section 103-1 to n adds the signal selected by the switch 101 and a replica signal of the pilot symbol output from a replica signal buffer 112 and performs despreading processing. Details of the internal configuration of the despreading sections 103-1 to n will be given later.

Each of discrimination circuits 104-1 to n makes a hard decision for each despread symbol. Then, discrimination circuits 104-1 to n output a pilot symbol following hard decision to a respreader 109, and output a data symbol after hard decision to corresponding likelihood calculators 105-1 to n and a decided value buffer 106.

Likelihood calculators 105-1 to n calculate the likelihood of the data symbols output from the corresponding despreading sections 103-1 to n and the data symbols output from the corresponding discrimination circuits 104-1 to n—that is, the data symbols before and after hard decision—for all data symbols present in a unit period (for example, a one-slot period), and output

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a signal indicating the likelihood to a likelihood buffer
107.

The decided value buffer 106 stores data symbols after hard decisions, and, based on a signal output by a ranking decision unit 108, outputs the data symbol after hard decision with the highest likelihood as a demodulated data symbol, and also outputs it to the resreader 109.

Based on the likelihoods stored in the information usage section 107, the ranking decision unit 108 attaches a rank to all undemodulated data symbols (hereinafter, processing for attaching a rank to all undemodulated symbols is referred to as "ranking processing"), and outputs a signal indicating the data symbol with the highest likelihood to the decided value buffer 106 and resreader 109.

The resreader 109 performs resreading by multiplying a pilot symbol after a hard decision by the channel estimate h_a , and outputs a pilot symbol after resreading to the replica signal buffer 112. In addition, the resreader 109 recognizes a demodulated data symbol output from the decided value buffer 106 based on a signal output from the ranking decision unit 108, performs resreading by multiplying the demodulated data symbol by the channel estimate h_a , and outputs a data symbol after resreading to a counter 110 and the subtracter 111.

The counter 110 counts the number of data symbols respread by the respreader 109—that is, the number of

demodulated data symbols—and when the count reaches a preset threshold value, outputs a signal indicating the processing start timing to despreading sections 103-1 to n. For example, if the threshold value is 3, the counter 5 110 outputs a timing signal at the point at which three data symbols have been demodulated.

The subtracter 111 subtracts the respread data symbols from the received signal output from the delayer 102, and outputs the signal after subtraction processing 10 to the switch 101.

The replica signal buffer 112 temporarily stores the respread pilot symbols, and outputs them to despreading sections 103-1 to n.

Next, the internal configuration of despreading 15 sections 103-1 to n will be described using the block diagram shown in FIG.3. As despreading sections 103-1 to n all have the same configuration, only the configuration of despreading section 103-1 for user 1 will be described here.

20 Adder 201-1 adds the signal selected by the switch 101 and the replica signal of the pilot symbol output from the replica signal buffer 112.

Matched filter 202-1 detects the correlation between the output signal from adder 201-1 and the 25 spreading code assigned to user 1. The correlation value detected by matched filter 202-1 is input to delay profile creator 203-1, channel estimate calculator 204-1, and RAKE combiner 205-1.

When a timing signal output from the counter 110 is input, delay profile creator 203-1 updates the delay profile, estimates the reception timing for each path by determining a threshold value with respect to the correlation value, and outputs a signal indicating the reception timing of each path to RAKE combiner 205-1 and resreader 109-1. For example, if the threshold value is 3, delay profile creator 203-1 inputs a timing signal at the point at which three data symbols have been demodulated, creates a delay profile and estimates the reception timing. By controlling the timing of delay profile updating, it is possible to achieve a balance between the precision of reception timing estimation and the amount of computation.

When a timing signal output from the counter 110 is input, channel estimate calculator 204-1 calculates channel estimate h_a for each pass, outputs channel estimate conjugate complex number h_a^* to RAKE combiner 205-1, and outputs channel estimate h_a to the resreader 109. For example, if the threshold value is 3, channel estimate calculator 204-1 inputs a timing signal at the point at which three data symbols have been demodulated, and calculates the channel estimate. By controlling the timing of channel estimate updating, it is possible to achieve a balance between channel estimate precision and the amount of computation.

RAKE combiner 205-1 multiplies the correlation value by channel estimate conjugate complex number h_a^*

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to compensate for channel fluctuations, and performs RAKE combination in symbol units based on the reception timing of each path, thereby improving quality. RAKE combiner 205-1 then outputs symbols after RAKE combination to discrimination circuit 104-1 and likelihood calculator 105-1.

When the reception timing of each path is newly detected by delay profile creator 203-1, and channel estimates are newly calculated by channel estimate calculator 204-1, RAKE combiner 205-1 performs processing using the updated path reception timings and channel estimates.

It is also possible for the timing for estimating reception timings by delay profile creation by delay profile creator 203-1 and the timing for channel estimate calculate by channel estimate calculator 204-1 to be made different.

Next, the flow of pilot symbol processing in the above-described receiving apparatus will be described.

Pilot symbols that have undergone RAKE combination by RAKE combiners 205-1 to n are output to discrimination circuits 104-1 to n and likelihood calculators 105-1 to n respectively.

Pilot symbols that have undergone RAKE combination undergo hard decision by discrimination circuits 104-1 to n and are output to the resreader 109.

Pilot symbols that have undergone hard decision are respread by means of multiplying spreading codes in the

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same way as on the transmitting side by the resreader 109, and pilot symbol replica signals are generated and output to the replica signal buffer 112.

After being stored temporarily in the replica signal
 5 buffer 112, pilot symbol replica signals are output to despread sections 103-1 to n, and in despread sections 103-1 to n, they are added to a signal with demodulated data symbols removed from the received signal, and correlation value detection, channel estimate
 10 calculation, and RAKE combination are performed.

The above-described series of processing steps for pilot symbols are then repeated until all the data symbols have been demodulated.

Next, the flow of data symbol processing in the
 15 above-described receiving apparatus will be described.

Data symbols that have undergone RAKE combination by RAKE combiners 205-1 to n are output to discrimination circuits 104-1 to n and likelihood calculators 105-1 to n respectively.

20 Data symbols that have undergone RAKE combination undergo hard decision by discrimination circuits 104-1 to and are output to likelihood calculators 105-1 to n.

After hard decision, data symbols are output respectively to likelihood calculators 105-1 to n and
 25 to the decided value buffer 106. Post-hard-decision data symbols are stored temporarily in the decided value buffer 106.

Meanwhile pre-hard-decision symbols output from

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5 105-1 to n. The likelihoods are stored temporarily in
the likelihood buffer 107.

10 symbol with the highest likelihood is output to the decided
value buffer 106 and resreader 109.

15 the drawing as a demodulated data symbol, as well as being
output to the resreader 109.

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20  replica signal is generated and output to the subtracter
    111.

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despreading sections 103-1 to n, and in despreading sections 103-1 to n is added to a pilot symbol replica signal, and then correlation value detection, channel estimate detection, and RAKE combination are performed.

The above-described series of processing steps are then repeated until all the data symbols have been demodulated.

By thus removing the pilot symbol and demodulated
5 data symbol replica signal from a received signal, and
using a signal to which a pilot symbol replica signal
has been added, it is possible to update and create a
delay profile, and to estimate reception timings with
high precision, and achieve an improvement in reception
10 quality sequentially.

(Embodiment 2)

FIG.4 is a block diagram showing the configuration of a receiving apparatus according to Embodiment 2. Parts of the receiving apparatus shown in FIG.4 identical to those in the receiving apparatus shown in FIG.2 are assigned the same reference numerals as in FIG.2 and their detailed explanations are omitted.

Compared with the receiving apparatus shown in FIG. 2, the configuration of the receiving apparatus in FIG. 4 has the addition of a pilot symbol buffer 301.

The pilot symbol buffer 301 stores pilot symbols.

Discrimination circuits 104-1 to n make a hard decision for each despread symbol. Then post-hard-decision data symbols are output to the corresponding likelihood calculators 105-1 to n and the decided value buffer 106.

The resreader 109 multiplies pilot symbols stored in the pilot symbol buffer 301 by channel estimate ha

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case is described where only the symbol with the highest likelihood is demodulated in one ranking processing operation, but the present invention is not limited to this, and can also be applied to a case where a plurality
5 of data symbols are demodulated in one ranking processing operation.

Furthermore, in the above-described embodiments, a case is described where symbol replica signals are created and eliminated, but the present invention is not
10 limited to this, and can also be applied to a case where an interference signal elimination apparatus is used.

As can be seen from the above descriptions, according to a receiving apparatus and reception timing estimation method of the present invention, it is possible to update
15 a delay profile and estimate reception timings with high precision, and to improve reception quality.

This application is based on the Japanese Patent Application No.2000-016161 filed on January 25, 2000, entire content of which is expressly incorporated by
20 reference herein.

Industrial Applicability

The present invention is suitable for use in a base station apparatus of a CDMA mobile communication system.